OIPE IAP20 DEC 10 2007 PATENT & TRADEMARK OFFICE

cofc

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | | |
|---|---|---|---|
| Patent | **7,068,672** | Grant Date | June 27, 2007 |
| First Inventor | James W. Jones | Filing Date | June 4, 2001 |
| Appl. No. | 09/874,395 | Confirmation No. | 4480 |
| Title: | ASYNCHRONOUS RECEIVE AND TRANSMIT PATCH CROSSPOINT | | |
| Docket No.: | CLX021 US | Customer No.: | 34036 |

Saratoga, California
December 5, 2007

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

**REQUEST FOR CERTIFICATE OF CORRECTION**

Dear Sir:

Errors appear in the above-identified patent and need to be corrected as shown in the attached proposed "CERTIFICATE OF CORRECTION." Specifically, on the front page of the printed patent under the heading "References Cited, U.S. PATENT DOCUMENTS", there are twenty-five (25) references missing for which the Examiner initialed as being considered during the prosecution of the application, in addition to OTHER PUBLICATIONS, of which there an additional twenty-seven (27) references missing for which the Examiner initialed as being considered during the prosecution of the application. See the attached copy of the Information Disclosure Statement by Applicant which was initialed by the Examiner. Hence a certificate of correction is hereby requested, pursuant to 35 USC § 254, 37 CFR 1.322 and MPEP 1480.

These errors appear to be made by the USPTO and hence no fee is believed to be needed. If any fee is deemed to be necessary, please charge the fee to the Deposit Account 50-2263 while citing to the Attorney Docket No. CLX021 US. Should there be any questions concerning this submission, please call the undersigned at (408) 378-7777, ext. 113

**CERTIFICATE OF MAILING BY "FIRST CLASS"**

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

S. Omkar — Dec 5, 2007
Attorney for Applicant(s) — Date of Signature

Respectfully submitted,

Certificate
DEC 13 2007
of Correction

S. Omkar

Omkar K. Suryadevara
Attorney for Applicants and Assignee
Reg. No. 36,320

DEC 13 2007

PTO/SB/44 (09-07) Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION



PATENT NO..: 7,068,672 B1

APPLICATION NO.: 09/874,395

ISSUE DATE: June 27, 2007

INVENTOR(S): James W. Jones

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

(56) References Cited

Please insert the following U.S. PATENT DOCUMENTS:

| | | |
|---|---|---|
| 5,119,367 | 06-1992 | Kawakatsu et al. |
| 5,295,135 | 03-1994 | Kammerl, Anton |
| 5,365,521 | 11-1994 | Ohnishi et al. |
| 5,455,826 | 10-1995 | Ozveren et al. |
| 5,500,858 | 03-1996 | McKeown |
| 5,577,035 | 11-1996 | Hayter et al. |
| 5,604,867 | 02-1997 | Harwood, Michael J. |
| 5,710,549 | 10-1998 | Horst et al. |
| 5,781,320 | 07-1998 | Byers, Charles Calvin |
| 5,923,644 | 07-1999 | McKeown et al. |
| 5,982,771 | 11/09/1999 | Caldara et al. |
| 5,987,026 | 11-1999 | Holland, Peter |
| 6,014,367 | 01-2000 | Joffe |
| 6,014,431 | 01-2000 | McHale et al. |
| 6,072,800 | 06-2000 | Lee |
| 6,134,217 | 10-2000 | Stiliadis et al. |
| 6,160,812 | 12-2000 | Bauman et al. |
| 6,181,694 | 01-2001 | Pickett, Scott K. |
| 6,195,355 | 02-2001 | Demizu |
| 6,262,986 | 07-2001 | Oba et al. |
| 6,327,253 | 12-2001 | Frink |
| 6,385,678 | 02-2002 | Jacobs et al. |
| 6,389,480 | 05-2002 | Kotzur et al. |
| 6,501,731 | 12-2002 | Chong et al. |
| 6,798,784 | 09-2004 | Dove et al. |

continued....

MAILING ADDRESS OF SENDER:

Silicon Valley Patent Group LLP
18805 Cox Avenue, Suite 220
Saratoga, CA 95070

PATENT NO. 7,246,043 B2

No. of additional copies

⇨ 0

DEC 13 2007

PTO/SB/44 (09-07) Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION



PATENT NO..: 7,068,672 B1
APPLICATION NO.: 09/874,395
ISSUE DATE: June 27, 2007
INVENTOR(S): James W. Jones

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

(56) References Cited

Please insert the following OTHER PUBLICATIONS:

PCT/US02/17515 PCT Search Report, dated 12 Dec. 2002, 1 pg;

PCT/US02/17515 Int'l Preliminary Examination Report, dated 12 Nov. 2003, 7 pgs;

Office Action dated September 28, 2004, (US Patent Application 10/199,996) (8 pages)

Response to Amendment dated September 28, 2004, (US Patent Application 10/199,996), filed January 24, 2005, (8 pages);

Office Action dated September 28, 2004 in EP Application No. 03254534.5-2416 based on US Patent Application 10/199,996 (5 pages total excluding cover sheet);

Search Report dated October 15, 2003 in EP Application No. 03254534.5-2416 based on US Patent Application 10/199,996 (2 pages total excluding cover sheet);

"The iSLIP scheduling algorithm for input-queued switches," by N. W. McKeown in IEEE/ACM Transactions on Networking, vol. 7, no. 2, April 1999;

T. Anderson, S. Owicki, J. Saxe and C. Thacker, "High Speed Switch for Local Area Networks", ACM Transactions on Computer Systems, vol. 11, no. 4, Nov. 1993 pp. 1-13;

N. W. McKeown, M. Izzard, A. Mekkittikul, W. Ellersick and M. Horowitz, "The tiny tera: A packet switch core", Hot Interconnects V., August 1996, pp. 1-13;

continued....

MAILING ADDRESS OF SENDER:

Silicon Valley Patent Group LLP
18805 Cox Avenue, Suite 220
Saratoga, CA 95070

PATENT NO. 7,246,043 B2

No. of additional copies
⇨ 0

DEC 13 2007

PTO/SB/44 (09-07) Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION



PATENT NO..: 7,068,672 B1

APPLICATION NO.: 09/874,395

ISSUE DATE: June 27, 2007

INVENTOR(S): James W. Jones

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

(56) References Cited

Please insert the following OTHER PUBLICATIONS:

A. Parekh, R. Gallager, "A Generalized Processor Sharing Approach To Flow Control in Integrated Services Networks: The Multiple Node Case", IEEE/ACM Transaction On Networking, VOL. 2, NO. 2, APRIIL 1994, pp. 136-151;

A. Parekh, R. Gallager, "A Generalized Processor Sharing Approach To Flow Control in Integrated Services Networks: The Single Node Case", IEEE/ACM Transaction On Networking, Vol. 1, No. 2, JUNE 1993, pp. 344-357;

D. Stiliadis, A. Varma, "Efficient Fair-Queueing Algorithms for Packet-Switched Networks", IEE/ACM Transaction On Networking, Vol. 6, No. 2, 1998, Article No. 27473, pp. 1-11 and B.1-B.2;

M. Goureau, S. Kolliopoulos, S. Rao, "Scheduling Algorithms for Input-Queued Switches: Randomized Techniques and Experimental Evaluation", IEEE/Infocom 2000, pp. 1634-1643;

J. Bennett, Hui Zhang "Why WFQ Is Not Good Enough For Integrated Services Networks", 1996, pp. 1-8;

N. McKeown, A. Mekkittikul, V. Anantharam, J. Walrand, "Achieving 100% Throughput in an Input-Queued Switch", IEEE Transaction Communications, Vol. 47, No. 8, August 1999, (22 pages);

I. Stoica, S. Shenker, H. Zhang, "Core-Stateless Fair Queueing: Achieving Approximately Fair Bandwidth Allocations in High Speed Networks", Http://www-2.cs.cmu.edu/~istoica/sig98talk/, 1998, pp1-20;

N. KcKeown, "Scheduling Algorithms for Input-Queued Cell Switches", © 1995, pp. 1-119;

R. Schoenen, "An Architecture Supporting Quality-of-Service in Virtual-Output-Queued Switches", iEICE Transaction Communications, Vol. E83-B, No. 2, February 2000, pp. 1-10

continued....

MAILING ADDRESS OF SENDER:

Silicon Valley Patent Group LLP
18805 Cox Avenue, Suite 220
Saratoga, CA 95070

PATENT NO. 7,246,043 B2

No. of additional copies

⇨ 0

DEC 19 2007

PTO/SB/44 (09-07) Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION



PATENT NO..: 7,068,672 B1

APPLICATION NO.: 09/874,395

ISSUE DATE: June 27, 2007

INVENTOR(S): James W. Jones

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

(56) References Cited

Please insert the following OTHER PUBLICATIONS:

M.J.G. van Uitert, S.C. Borst, "A Reduced-Load Equivalence For Generalized Processor Sharing Networks With Heavy-Tailed Input Flows", Probability, Networks and Algorithms (PNA), PNA-R007, August 31, 2000, pp. 1-37;

N. Joy, K. Jamadagni, "Optimal Call Admission Control in Generalized Processor Sharing (GPS) Schedulers", IEEE Infocom 2001, pp. 1-10;

D. Stiliadis, A. Varma, "Rate-Proportional Servers: A Design Methodology for Fair Queueing Algorithms", UCSC-CRL-95-58, December 1995, pp. 1-22 and A.1-A.4;

D. Staliadis, A. Varma, "Latency-Rate Servers: A General Model for Analysis of Traffic Scheduling Algoriths", IEEE/ACM Transactions of Networking, Vol. 6, No. 5, October 1998, pp. 611-624;

M. Vishnu, "Implementing VirtualClock without Cell Stamps", IEEE Communications Letters, 1997, pp. 1-3;

M. Vishnu, J. Mark, "A Flexible Service Scheduling Scheme for ATM Networks", DBLP Record 'conf/infocom/VishnuM96, 1996, pp. 647-654;

M. Vishnu, J. Mark, "Reference Queue Tracking Strategies for Delay Guarantees in ATM Networks", November 4, 1997, pp. 1-22;

M. Vishnu, J. Mark, "Reference Queue Tracking Strategies for Delay Guarantees in ATM Networks", November 22, 1999, pp. 1-18;

M. Vishnu, J. Mark, "HOL-EDD: A Novel Service Scheduling Scheme for ATM Networks", June 16, 1997, pp. 1-23.

MAILING ADDRESS OF SENDER:

Silicon Valley Patent Group LLP
18805 Cox Avenue, Suite 220
Saratoga, CA 95070

PATENT NO. 7,246,043 B2

No. of additional copies

⇨ 0

DEC 13 2007

IDS: 3/15/05



U.S. Department of Commerce, Patent and Trademark Office

OIPE
MAR 15 2005
PATENT & TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

| | |
|---|---|
| Application No.: | 09/874,402 |
| Filing Date: | June 4, 2001 |
| First Named Inventor: | Jason Dove |
| Group Art Unit: | 2662 |
| Examiner Name: | Unknown |
| Confirmation No.: | 4498 |
| Attorney Docket No.: | CLX023 US |

U.S. Patent Documents

| *Examiner Intials | | Document Number | Date | Name | Class | Subclass | Filing Date if Appropriate |
|---|---|---|---|---|---|---|---|
| | 1. | 6,195,355 | 02/2001 | Demizu | 370 | 397 | |
| | 2. | 6,181,694 | 01/2001 | Pickett, Scott K. | 370 | 458 | |
| | 3. | 5,987,026 | 11/1999 | Holland, Peter | 370 | 353 | |
| | 4. | 6,014,431 | 01/2000 | McHale et al. | 379 | 93.07 | |
| | 5. | 5,365,521 | 11/1994 | Ohnishi et al. | 370 | 352 | |
| | 6. | 5,781,320 | 07/1998 | Byers, Charles Calvin | 370 | 395.51 | |
| | 7. | 6,798,784 | 09/2004 | Dove et al. | 370 | 463 | |
| | 8. | 6,262,986 | Jul-01 | Oba et al. | 370 | 399 | |
| | 9. | 6,072,800 | Jun-00 | Lee | 370 | 412 | |
| | 10. | 6,014,367 | Jan-00 | Joffe | 370 | 230 | |
| | 11. | 5,455,826 | Oct-95 | Ozveren et al. | 370 | 60 | |
| | 12. | 5,577,035 | Nov-96 | Hayter et al. | 370 | 60 | |
| | 13. | 5,500,858 | Mar-96 | McKeown | 370 | 60 | |
| | 14. | 5,923,644 | Jul-99 | McKeown et al. | 370 | 230 | |
| | 15. | 6,160,812 | Dec-00 | Bauman et al. | 370 | 416 | |
| | 16. | 6,327,253 | Dec-01 | Frink | 370 | 260 | |
| | 17. | 6,134,217 | Oct-00 | Stiliadis et al. | 370 | 232 | |
| | 18. | 5,982,771 | 9 Nov. 1999 | Caldara et al. | 370 | 389 | |
| | 19. | 6,501,731 | Dec-02 | Chong et al. | 370 | 230.1 | |
| | 20. | 6,389,480 | May-02 | Kotzur et al. | 709 | 249 | |
| | 21. | 5,604,867 | Feb-97 | Harwood, Michael J. | 709 | 233 | |
| | 22. | 6,385,678 | Feb-02 | Jacobs et al. | 710 | 113 | |
| | 23. | 5,119,367 | Jun-92 | Kawakatsu et al. | 370 | 232 | |
| | 24. | 5,710,549 | Jan-98 | Horst et al. | 340 | 825.5 | |
| | 25. | 5,295,135 | Mar-94 | Kammerl, Anton | 370 | 233 | |

Examiner: Hoa T. Nguyen

Date Considered: 5/05/05

* Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication with applicant.

DEC 13 2007

| U.S. Department of Commerce, Patent and Trademark Office | Application No.: | 09/874,402 |
|---|---|---|
| | Filing Date: | June 4, 2001 |
| | First Named Inventor: | Jason Dove |
| | Group Art Unit: | 2662 |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | Examiner Name: | Unknown |
| (Use several sheets if necessary) | Confirmation No.: | 4498 |
| | Attorney Docket No.: | CLX023 US |

OIPE MAR 15 2005 PATENT & TRADEMARK OFFICE

| Other Art (Including Author, Title, Date, Pertinent Pages, Etc.) | | |
|---|---|---|
| | 26. | PCT/US02/17515 PCT Search Report, dated 12 Dec. 2002, 1 page |
| | 27. | PCT/US02/17515 Int'l Preliminary Examination Report, dated 12 Nov. 2003, 7 pages |
| | 28. | Office Action dated September 28, 2004, (US Patent Application 10/199,996) (8 pages) |
| | 29. | Response to Amendment dated September 28, 2004, (US Patent Application 10/199,996), filed January 24, 2005, (8 pages) |
| | 30. | Office Action dated September 28, 2004 in EP Application No. 03254534.5-2416 based on US Patent Application 10/199,996 (5 pages total excluding cover sheet) |
| | 31. | Search Report dated October 15, 2003 in EP Application No. 03254534.5-2416 based on US Patent Application 10/199,996 (2 pages total excluding cover sheet) |
| | 32. | "The iSLIP scheduling algorithm for input-queued switches," by N. W. McKeown in IEEE/ACM Transactions on Networking, vol. 7, no. 2, April 1999 |
| | 33. | T. Anderson, S. Owicki, J. Saxe and C. Thacker, "High Speed Switch for Local Area Networks", ACM Transactions on Computer Systems, vol. 11, no. 4, Nov. 1993 pp. 1-13 |
| | 34. | N. W. McKeown, M. Izzard, A. Mekkittikul, W. Ellersick and M. Horowitz, "The tiny tera: A packet switch core", Hot Interconnects V., August 1996, pp. 1-13 |
| | 35. | A. Parekh, R. Gallager, "A Generalized Processor Sharing Approach To Flow Control in Integrated Services Networks: The Multiple Node Case", IEEE/ACM Transaction On Networking, VOL. 2, NO. 2, APRIIL 1994, pp. 136-151 |
| | 36. | A. Parekh, R. Gallager, "A Generalized Processor Sharing Approach To Flow Control in Integrated Services Networks: The Single Node Case", IEEE/ACM Transaction On Networking, Vol. 1, No. 2, JUNE 1993, pp. 344-357 |
| | 37. | D. Stiliadis, A. Varma, "Efficient Fair-Queueing Algorithms for Packet-Switched Networks", IEE/ACM Transaction On Networking, Vol. 6, No. 2, 1998, Article No. 27473, pp. 1-11 and B.1-B.2 |
| | 38. | M. Goureau, S. Kolliopoulos, S. Rao, "Scheduling Algorithms for Input-Queued Switches: Randomized Techniques and Experimental Evaluation", IEEE/Infocom 2000, pp. 1634-1643 |
| | 39. | J. Bennett, Hui Zhang "Why WFQ Is Not Good Enough For Integrated Services Networks", 1996, pp. 1-8 |
| | 40. | N. McKeown, A. Mekkittikul, V. Ananthāram, J. Walrand, "Achieving 100% Throughput in an Input-Queued Switch", IEEE Transaction Communications, Vol. 47, No. 8, August 1999, (22 pages) |
| | 41. | I. Stoica, S. Shenker, H. Zhang, "Core-Stateless Fair Queueing: Achieving Approximately Fair Bandwidth Allocations in High Speed Networks", Http://www-2.cs.cmu.edu/~istoica/sig98talk/, 1998, pp1-20 |
| | 42. | N. KcKeown, "Scheduling Algorithms for Input-Queued Cell Switches", © 1995, pp. 1-119 |
| | 43. | R. Schoenen, "An Architecture Supporting Quality-of-Service in Virtual-Output-Queued Switches", iEICE Transaction Communications, Vol. E83-B, No. 2, February 2000, pp. 1-10 |
| | 44. | M.J.G. van Uitert, S.C. Borst, "A Reduced-Load Equivalence For Generalized Processor Sharing Networks With Heavy-Tailed Input Flows", Probability, Networks and Algorithms (PNA), PNA-R007, August 31, |

| Examiner: Mahtab Masud | Date Considered: 05/05/08 |
|---|---|

* Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication with applicant.

DEC 13 2007

| U.S. Department of Commerce, Patent and Trademark Office | Application No.: | 09/874,402 |
|---|---|---|
| | Filing Date: | June 4, 2001 |
| | First Named Inventor: | Jason Dove |
| | Group Art Unit: | 2662 |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | Examiner Name: | Unknown |
| (Use several sheets if necessary) | Confirmation No.: | 4498 |
| | Attorney Docket No.: | CLX023 US |

OIPE SC163 MAR 15 2005 PATENT & TRADEMARK OFFICE

| | | |
|---|---|---|
| | | 2000, pp. 1-37 |
| | 45. | N. Joy, K. Jamadagni, "Optimal Call Admission Control in Generalized Processor Sharing (GPS) Schedulers", IEEE Infocom 2001, pp. 1-10 |
| | 46. | D. Stiliadis, A. Varma, "Rate-Proportional Servers: A Design Methodology for Fair Queueing Algorithms", UCSC-CRL-95-58, December 1995, pp. 1-22 and A.1-A.4 |
| | 47. | D. Staliadis, A. Varma, "Latency-Rate Servers: A General Model for Analysis of Traffic Scheduling Algoriths", IEEE/ACM Transactions of Networking, Vol. 6, No. 5, October 1998, pp. 611-624 |
| | 48. | M. Vishnu, "Implementing VirtualClock without Cell Stamps", IEEE Communications Letters, 1997, pp. 1-3 |
| | 49. | M. Vishnu, J. Mark, "A Flexible Service Scheduling Scheme for ATM Networks", DBLP Record 'conf/infocom/VishnuM96, 1996, pp. 647-654 |
| | 50. | M. Vishnu, J. Mark, "Reference Queue Tracking Strategies for Delay Guarantees in ATM Networks", November 4, 1997, pp. 1-22 |
| | 51. | M. Vishnu, J. Mark, "Reference Queue Tracking Strategies for Delay Guarantees in ATM Networks", November 22, 1999, pp. 1-18 |
| | 52. | M. Vishnu, J. Mark, "HOL-EDD: A Novel Service Scheduling Scheme for ATM Networks", June 16, 1997, pp. 1-23 |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

| Examiner: | Date Considered: |
|---|---|
| | 08/07/08 |

* Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication with applicant.

DEC 13 2007

IDS: 3/15/05



U.S. Department of Commerce, Patent and Trademark Office

OIPE C163 MAR 15 2005 PATENT & TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

| | |
|---|---|
| Application No.: | 09/874,402 |
| Filing Date: | June 4, 2001 |
| First Named Inventor: | Jason Dove |
| Group Art Unit: | 2662 |
| Examiner Name: | Unknown |
| Confirmation No.: | 4498 |
| Attorney Docket No.: | CLX023 US |

U.S. Patent Documents

| *Examiner Intials | | Document Number | Date | Name | Class | Subclass | Filing Date if Appropriate |
|---|---|---|---|---|---|---|---|
| | 1. | 6,195,355 | 02/2001 | Demizu | 370 | 397 | |
| | 2. | 6,181,694 | 01/2001 | Pickett, Scott K. | 370 | 458 | |
| | 3. | 5,987,026 | 11/1999 | Holland, Peter | 370 | 353 | |
| | 4. | 6,014,431 | 01/2000 | McHale et al. | 379 | 93.07 | |
| | 5. | 5,365,521 | 11/1994 | Ohnishi et al. | 370 | 352 | |
| | 6. | 5,781,320 | 07/1998 | Byers, Charles Calvin | 370 | 395.51 | |
| | 7. | 6,798,784 | 09/2004 | Dove et al. | 370 | 463 | |
| | 8. | 6,262,986 | Jul-01 | Oba et al. | 370 | 399 | |
| | 9. | 6,072,800 | Jun-00 | Lee | 370 | 412 | |
| | 10. | 6,014,367 | Jan-00 | Joffe | 370 | 230 | |
| | 11. | 5,455,826 | Oct-95 | Ozveren et al. | 370 | 60 | |
| | 12. | 5,577,035 | Nov-96 | Hayter et al. | 370 | 60 | |
| | 13. | 5,500,858 | Mar-96 | McKeown | 370 | 60 | |
| | 14. | 5,923,644 | Jul-99 | McKeown et al. | 370 | 230 | |
| | 15. | 6,160,812 | Dec-00 | Bauman et al. | 370 | 416 | |
| | 16. | 6,327,253 | Dec-01 | Frink | 370 | 260 | |
| | 17. | 6,134,217 | Oct-00 | Stiliadis et al. | 370 | 232 | |
| | 18. | 5,982,771 | 9 Nov. 1999 | Caldara et al. | 370 | 389 | |
| | 19. | 6,501,731 | Dec-02 | Chong et al. | 370 | 230.1 | |
| | 20. | 6,389,480 | May-02 | Kotzur et al. | 709 | 249 | |
| | 21. | 5,604,867 | Feb-97 | Harwood, Michael J. | 709 | 233 | |
| | 22. | 6,385,678 | Feb-02 | Jacobs et al. | 710 | 113 | |
| | 23. | 5,119,367 | Jun-92 | Kawakatsu et al. | 370 | 232 | |
| | 24. | 5,710,549 | Jan-98 | Horst et al. | 340 | 825.5 | |
| | 25. | 5,295,135 | Mar-94 | Kammerl, Anton | 370 | 233 | |

| | |
|---|---|
| Examiner: | Date Considered: 5/05/05 |

* Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication with applicant.

DEC 13 2007

| U.S. Department of Commerce, Patent and Trademark Office | Application No.: | 09/874,402 |
|---|---|---|
| | Filing Date: | June 4, 2001 |
| | First Named Inventor: | Jason Dove |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | Group Art Unit: | 2662 |
| (Use several sheets if necessary) | Examiner Name: | Unknown |
| | Confirmation No.: | 4498 |
| | Attorney Docket No.: | CLX023 US |

OIPE MAR 15 2005 PATENT & TRADEMARK OFFICE

| Other Art (Including Author, Title, Date, Pertinent Pages, Etc.) | | |
|---|---|---|
| | 26. | PCT/US02/17515 PCT Search Report, dated 12 Dec. 2002, 1 page |
| | 27. | PCT/US02/17515 Int'l Preliminary Examination Report, dated 12 Nov. 2003, 7 pages |
| | 28. | Office Action dated September 28, 2004, (US Patent Application 10/199,996) (8 pages) |
| | 29. | Response to Amendment dated September 28, 2004, (US Patent Application 10/199,996), filed January 24, 2005, (8 pages) |
| | 30. | Office Action dated September 28, 2004 in EP Application No. 03254534.5-2416 based on US Patent Application 10/199,996 (5 pages total excluding cover sheet) |
| | 31. | Search Report dated October 15, 2003 in EP Application No. 03254534.5-2416 based on US Patent Application 10/199,996 (2 pages total excluding cover sheet) |
| | 32. | "The iSLIP scheduling algorithm for input-queued switches," by N. W. McKeown in IEEE/ACM Transactions on Networking, vol. 7, no. 2, April 1999 |
| | 33. | T. Anderson, S. Owicki, J. Saxe and C. Thacker, "High Speed Switch for Local Area Networks", ACM Transactions on Computer Systems, vol. 11, no. 4, Nov. 1993 pp. 1-13 |
| | 34. | N. W. McKeown, M. Izzard, A. Mekkittikul, W. Ellersick and M. Horowitz, "The tiny tera: A packet switch core", Hot Interconnects V., August 1996, pp. 1-13 |
| | 35. | A. Parekh, R. Gallager, "A Generalized Processor Sharing Approach To Flow Control in Integrated Services Networks: The Multiple Node Case", IEEE/ACM Transaction On Networking, VOL. 2, NO. 2, APRIIL 1994, pp. 136-151 |
| | 36. | A. Parekh, R. Gallager, "A Generalized Processor Sharing Approach To Flow Control in Integrated Services Networks: The Single Node Case", IEEE/ACM Transaction On Networking, Vol. 1, No. 2, JUNE 1993, pp. 344-357 |
| | 37. | D. Stiliadis, A. Varma, "Efficient Fair-Queueing Algorithms for Packet-Switched Networks", IEE/ACM Transaction On Networking, Vol. 6, No. 2, 1998, Article No. 27473, pp. 1-11 and B.1-B.2 |
| | 38. | M. Goureau, S. Kolliopoulos, S. Rao, "Scheduling Algorithms for Input-Queued Switches: Randomized Techniques and Experimental Evaluation", IEEE/Infocom 2000, pp. 1634-1643 |
| | 39. | J. Bennett, Hui Zhang "Why WFQ Is Not Good Enough For Integrated Services Networks", 1996, pp. 1-8 |
| | 40. | N. McKeown, A. Mekkittikul, V. Anantharam, J. Walrand, "Achieving 100% Throughput in an Input-Queued Switch", IEEE Transaction Communications, Vol. 47, No. 8, August 1999, (22 pages) |
| | 41. | I. Stoica, S. Shenker, H. Zhang, "Core-Stateless Fair Queueing: Achieving Approximately Fair Bandwidth Allocations in High Speed Networks", Http://www-2.cs.cmu.edu/~istoica/sig98talk/, 1998, pp1-20 |
| | 42. | N. KcKeown, "Scheduling Algorithms for Input-Queued Cell Switches", © 1995, pp. 1-119 |
| | 43. | R. Schoenen, "An Architecture Supporting Quality-of-Service in Virtual-Output-Queued Switches", iEICE Transaction Communications, Vol. E83-B, No. 2, February 2000, pp. 1-10 |
| | 44. | M.J.G. van Uitert, S.C. Borst, "A Reduced-Load Equivalence For Generalized Processor Sharing Networks With Heavy-Tailed Input Flows", Probability, Networks and Algorithms (PNA), PNA-R007, August 31, |

| Examiner: Mukta Mend | Date Considered: 05/05/08 |
|---|---|

* Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication with applicant.

DEC 13 2007

| U.S. Department of Commerce, Patent and Trademark Office | Application No.: | 09/874,402 |
|---|---|---|
| | Filing Date: | June 4, 2001 |
| | First Named Inventor: | Jason Dove |
| | Group Art Unit: | 2662 |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | Examiner Name: | Unknown |
| (Use several sheets if necessary) | Confirmation No.: | 4498 |
| | Attorney Docket No.: | CLX023 US |

RECEIVED JC163 MAR 15 2005 PATENT & TRADEMARK OFFICE

| | | |
|---|---|---|
| | | 2000, pp. 1-37 |
| | 45. | N. Joy, K. Jamadagni, "Optimal Call Admission Control in Generalized Processor Sharing (GPS) Schedulers", IEEE Infocom 2001, pp. 1-10 |
| | 46. | D. Stiliadis, A. Varma, "Rate-Proportional Servers: A Design Methodology for Fair Queueing Algorithms", UCSC-CRL-95-58, December 1995, pp. 1-22 and A.1-A.4 |
| | 47. | D. Staliadis, A. Varma, "Latency-Rate Servers: A General Model for Analysis of Traffic Scheduling Algoriths", IEEE/ACM Transactions of Networking, Vol. 6, No. 5, October 1998, pp. 611-624 |
| | 48. | M. Vishnu, "Implementing VirtualClock without Cell Stamps", IEEE Communications Letters, 1997, pp. 1-3 |
| | 49. | M. Vishnu, J. Mark, "A Flexible Service Scheduling Scheme for ATM Networks", DBLP Record 'conf/infocom/VishnuM96, 1996, pp. 647-654 |
| | 50. | M. Vishnu, J. Mark, "Reference Queue Tracking Strategies for Delay Guarantees in ATM Networks", November 4, 1997, pp. 1-22 |
| | 51. | M. Vishnu, J. Mark, "Reference Queue Tracking Strategies for Delay Guarantees in ATM Networks", November 22, 1999, pp. 1-18 |
| | 52. | M. Vishnu, J. Mark, "HOL-EDD: A Novel Service Scheduling Scheme for ATM Networks", June 16, 1997, pp. 1-23 |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

| Examiner: | Date Considered: |
|---|---|
| | |

* Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication with applicant.

DEC 13 2007